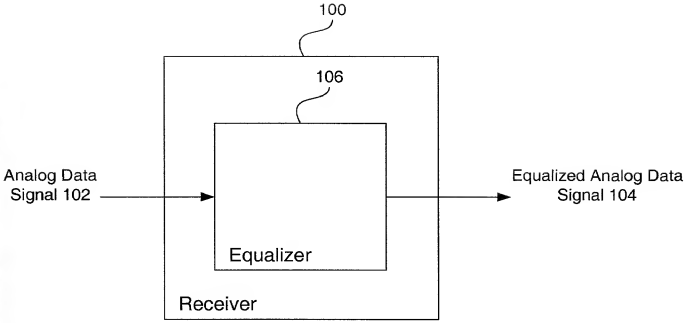

100
106
Analog Data
Signal 102
Equalizer
Receiver
Equalized Analog Data
Signal 104

FIG. 1

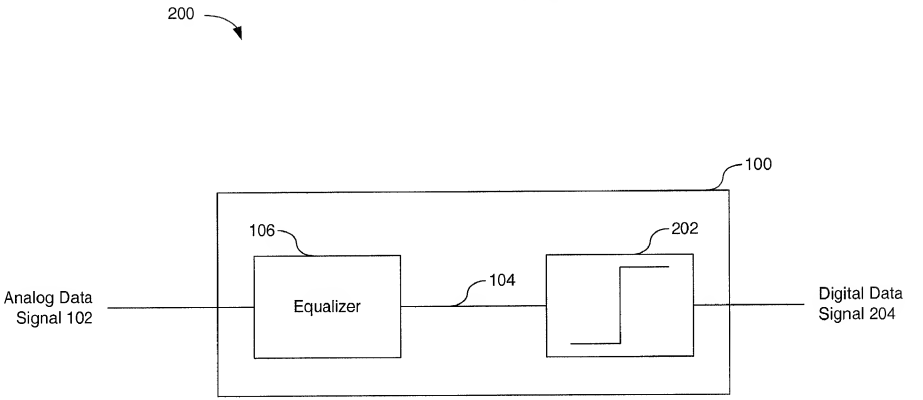
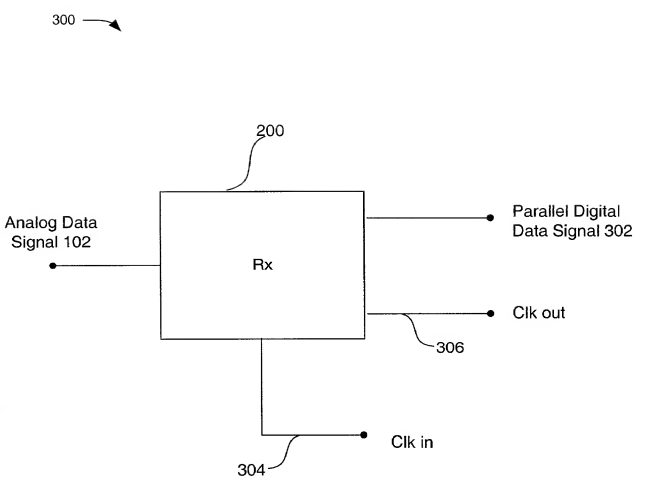

200
100
106
Equalizer
104
202
Analog Data
Signal 102
Digital Data
Signal 204

FIG. 2



Serial-to-Parallel Receiver

FIG. 3

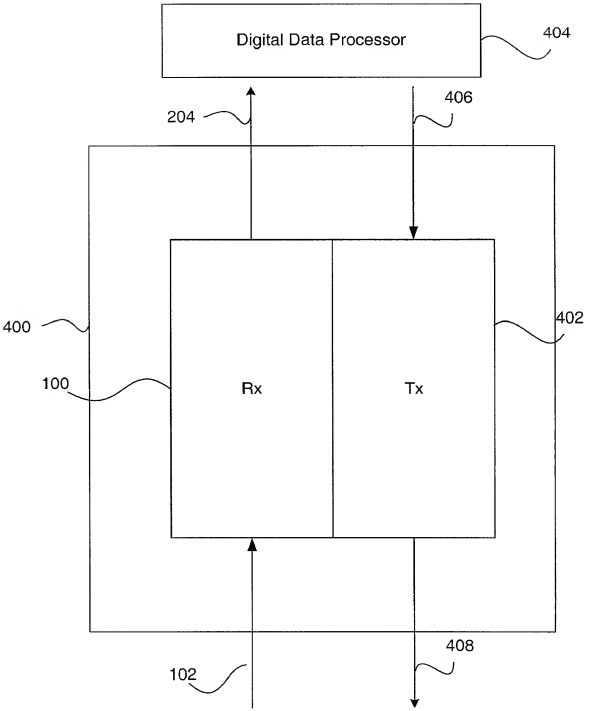


FIG. 4

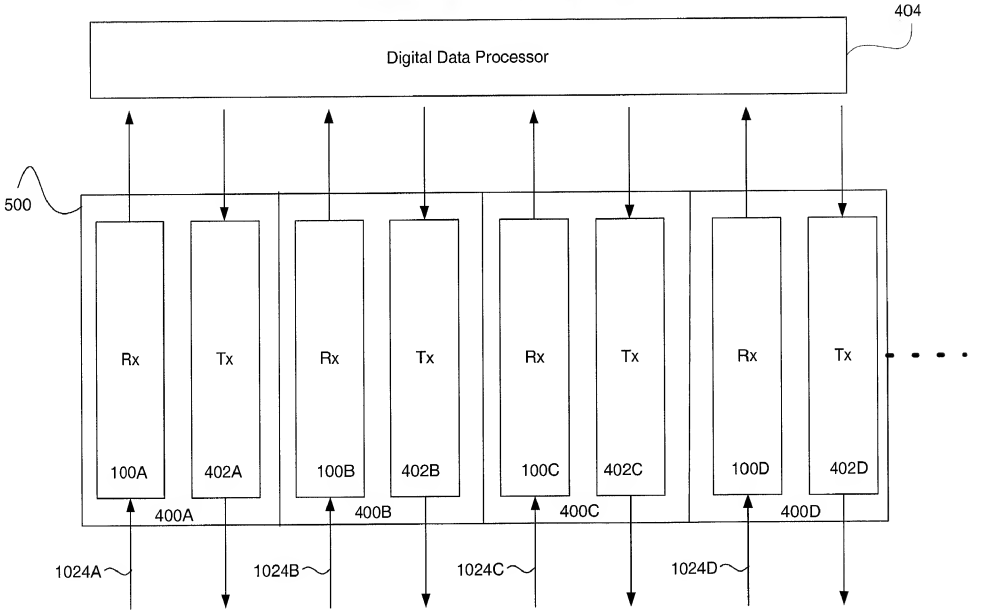


FIG. 5

0101-93.vsd/5

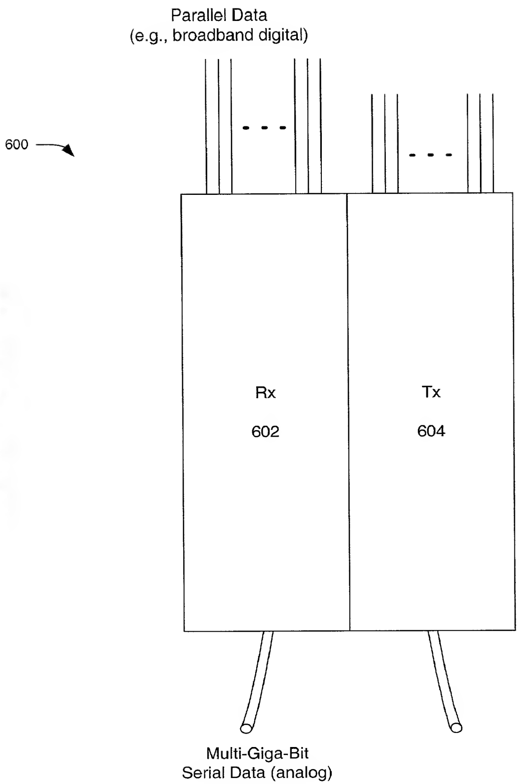

Parallel Data
(e.g., broadband digital)
600
Rx
602
Tx
604
Multi-Giga-Bit
Serial Data (analog)

FIG. 6

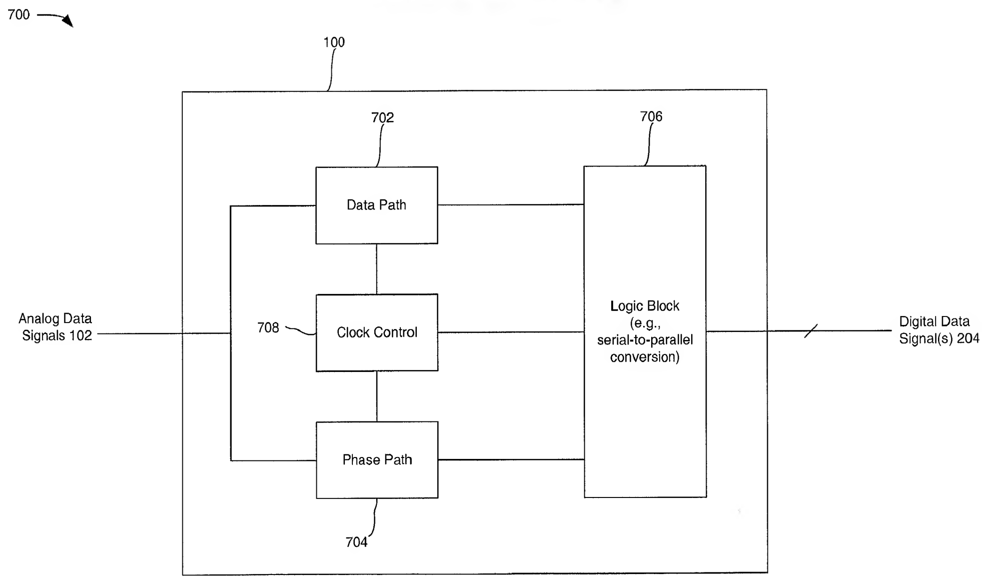


FIG. 7

0101-93.vsd/7

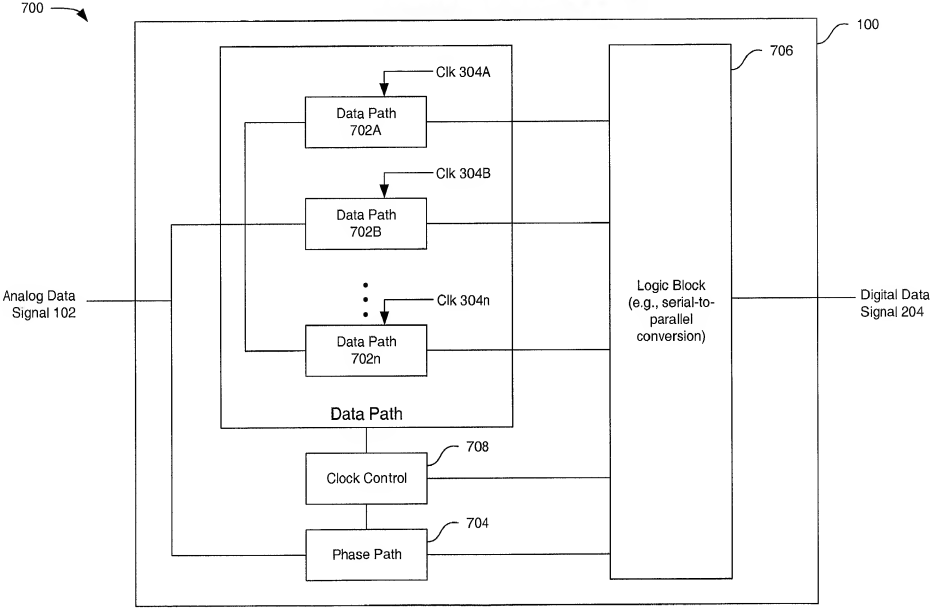


FIG. 8

0101-93.vsd/8

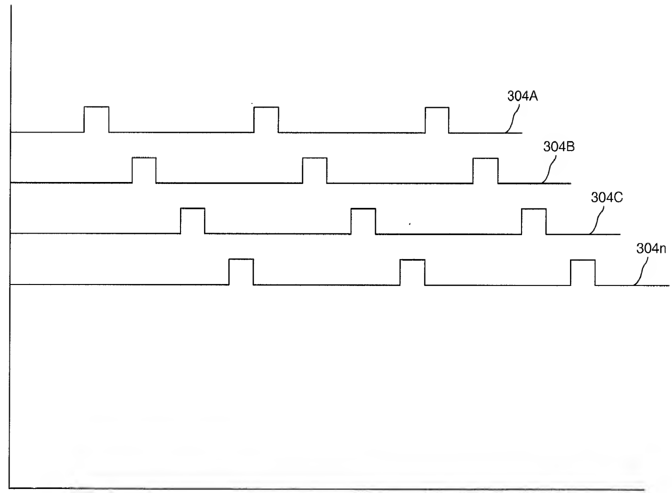


FIG. 9

0101-93.vsd/9

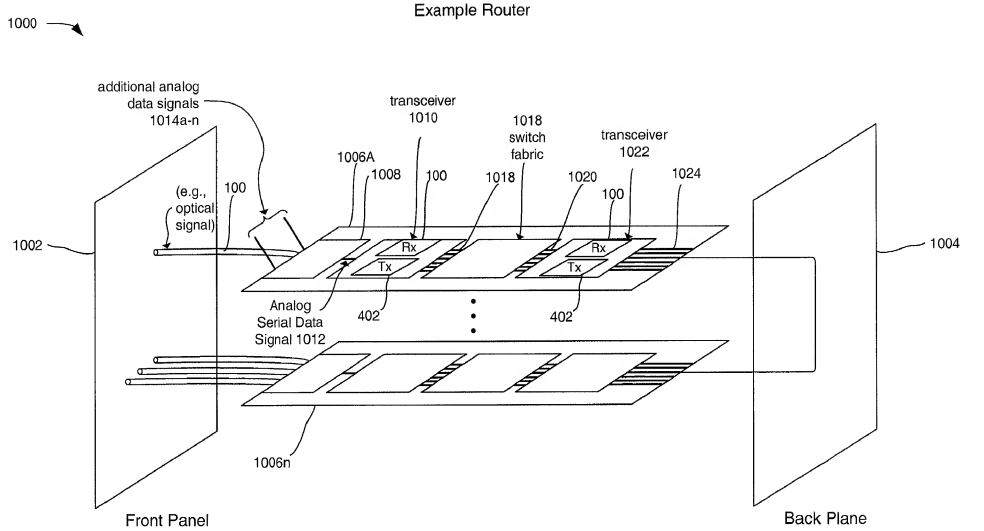


FIG. 10

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
No Equalization

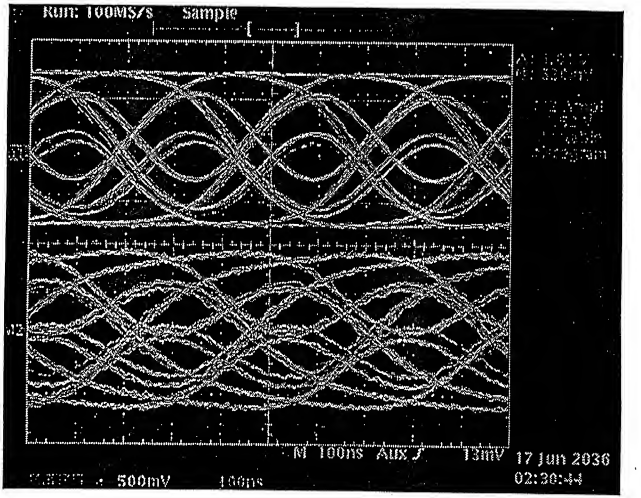


FIG. 11A

Firewire
25-feet IEEE 1394
No Equalization

FIG. 11B

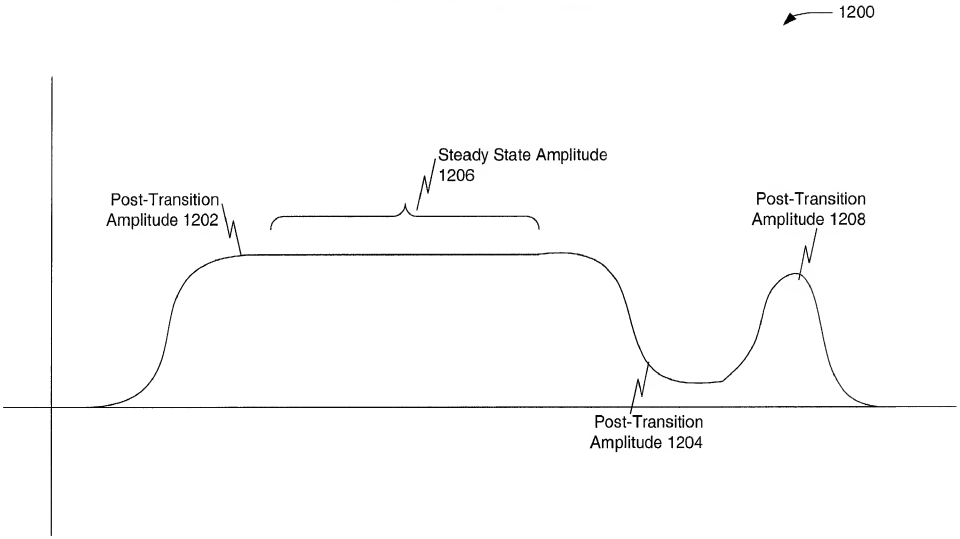

1200
Steady State Amplitude
1206
Post-Transition
Amplitude 1202
Post-Transition
Amplitude 1208
Post-Transition
Amplitude 1204

FIG. 12

Receiver Eye Diagrams: 3.125-Gb/s

Backplane
36-inches FR4
Equalization
a = 0.25
Eye Opening = 900mV

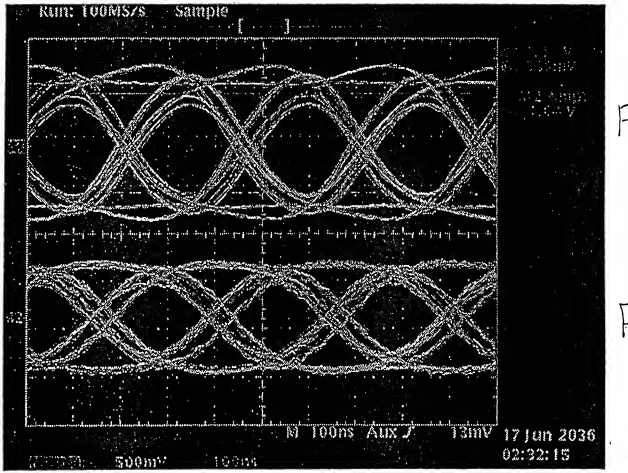


FIG 13A

Firewire
25-feet IEEE 1394
Equalization
a = 0.375
Eye Opening = 750mV

FIG. 13B

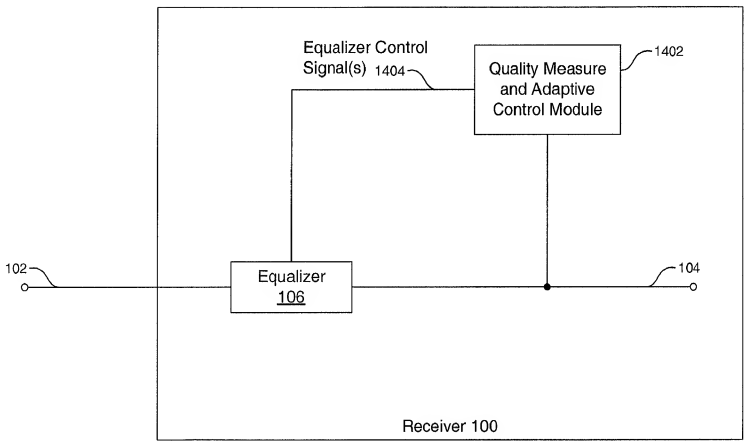


FIG. 14A

0101-93.vsd/12

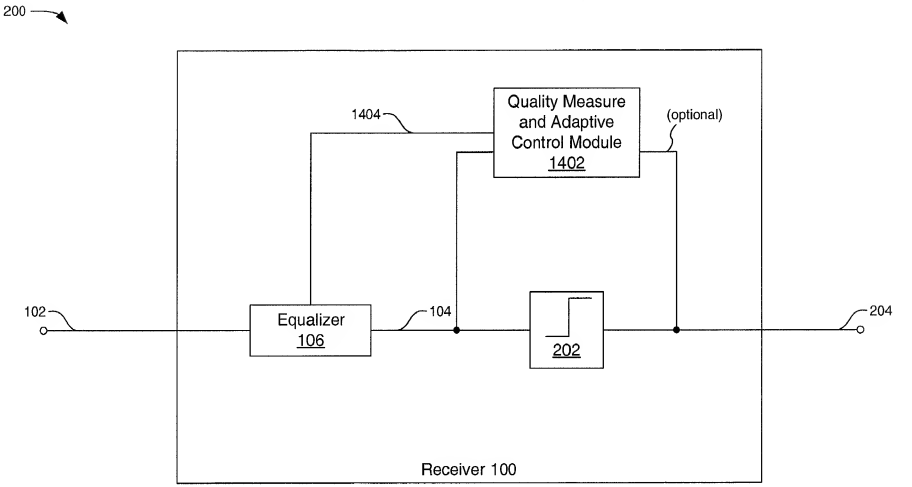


FIG. 14B

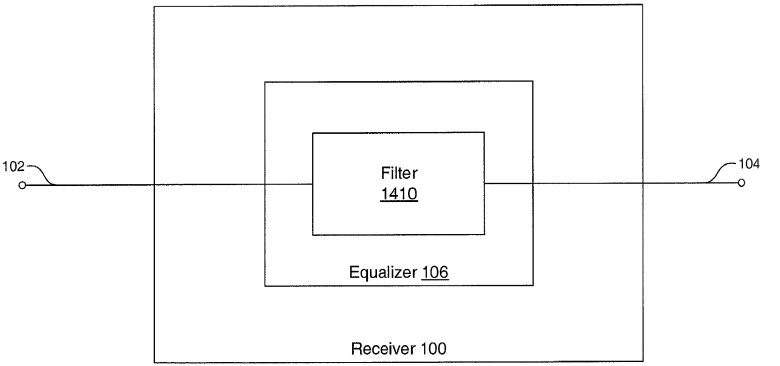


FIG. 14C

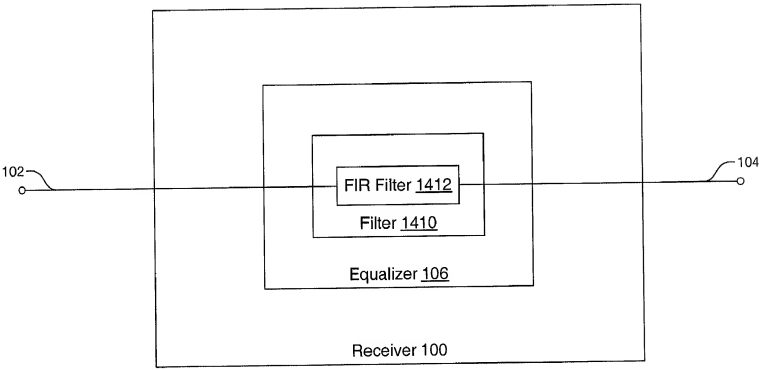

102
104
FIR Filter 1412
Filter 1410
Equalizer 106
Receiver 100

FIG. 14D

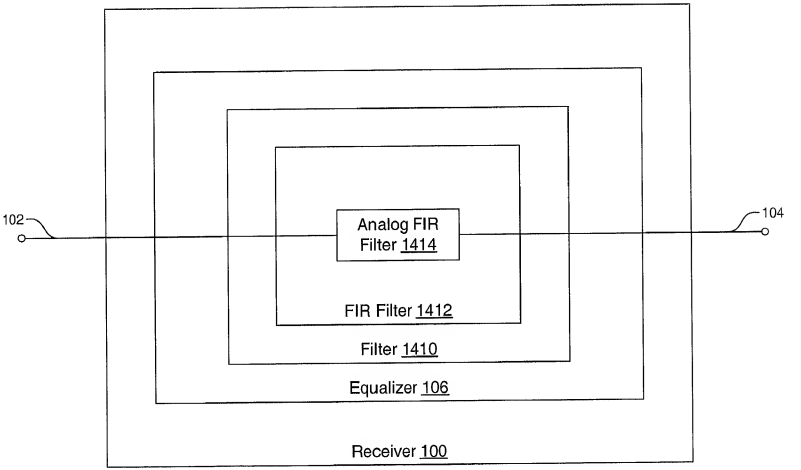


FIG. 14E

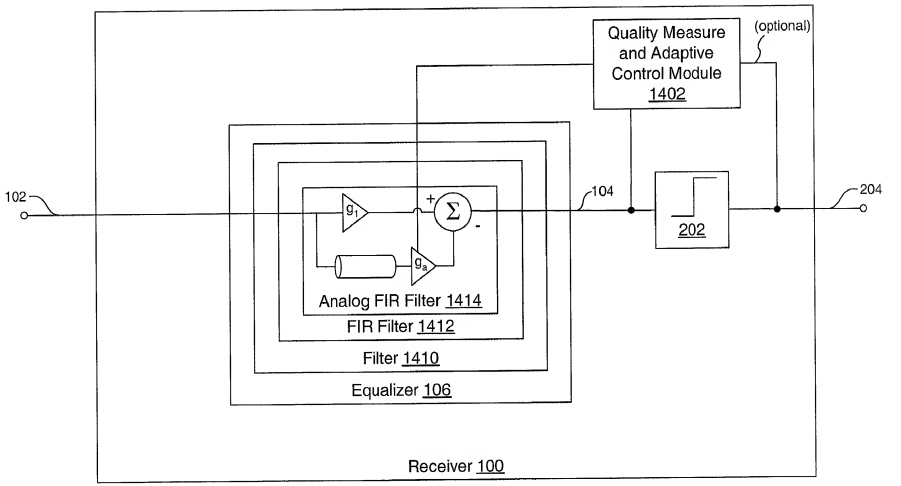


FIG. 14F

0101-93.vsd/17

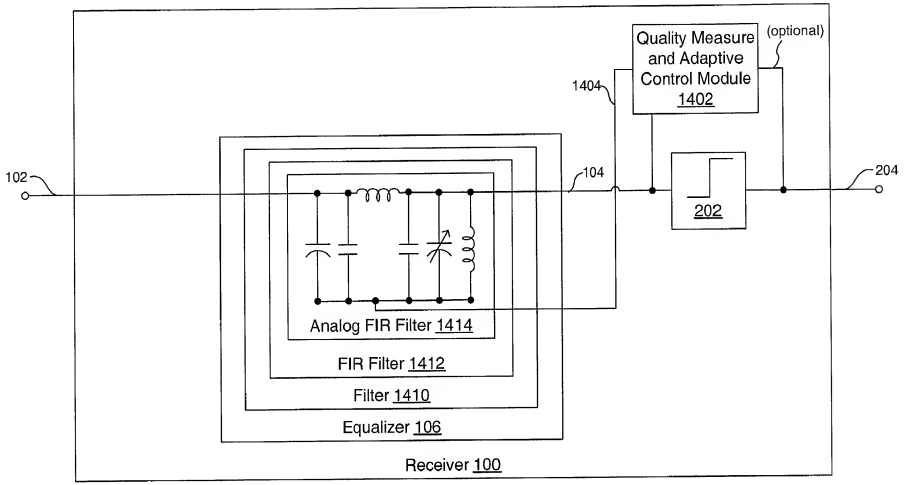


FIG. 14G

0101-93.vsd/18

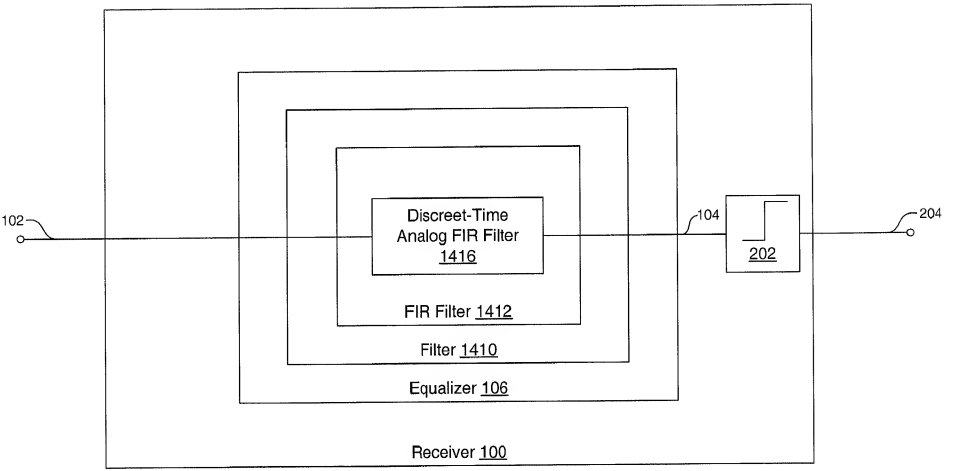


FIG. 14H

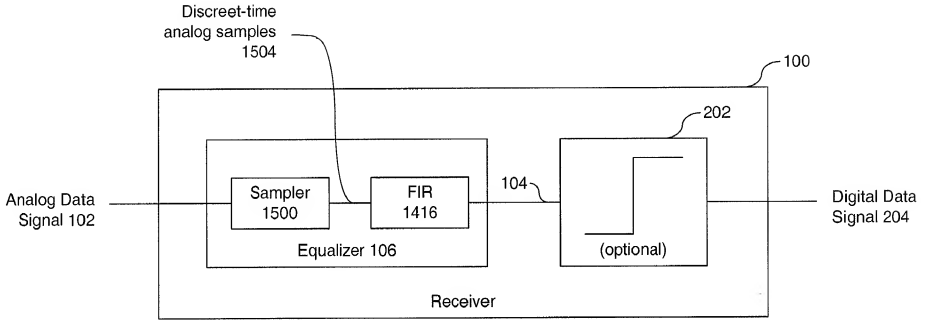


FIG. 15

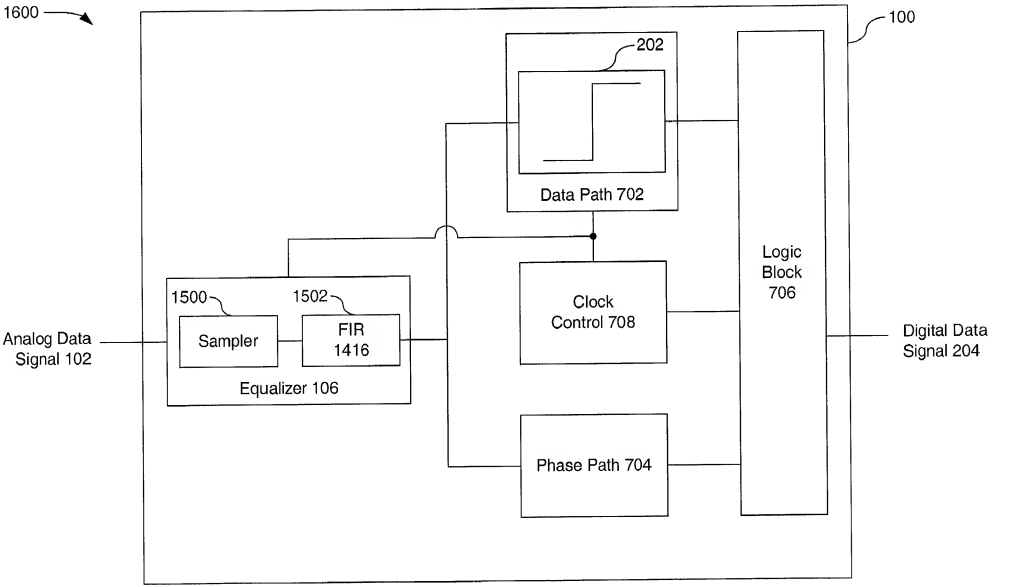


FIG. 16

0101-93.vsd/22

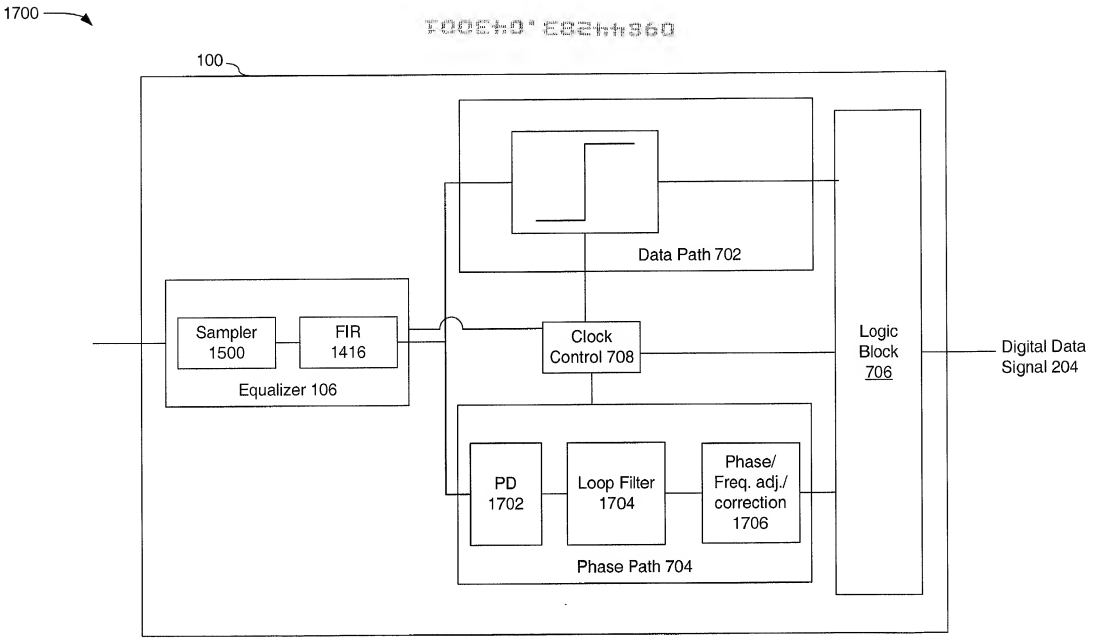


FIG. 17

0101-93.vsd/23

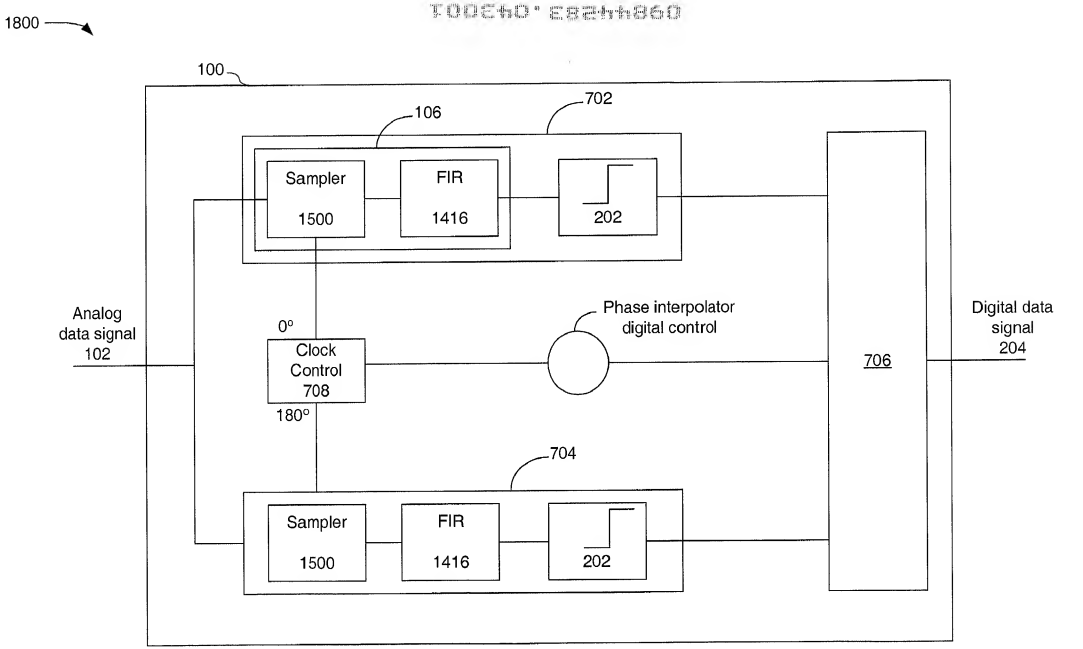


FIG. 18

0101-93.vsd/24

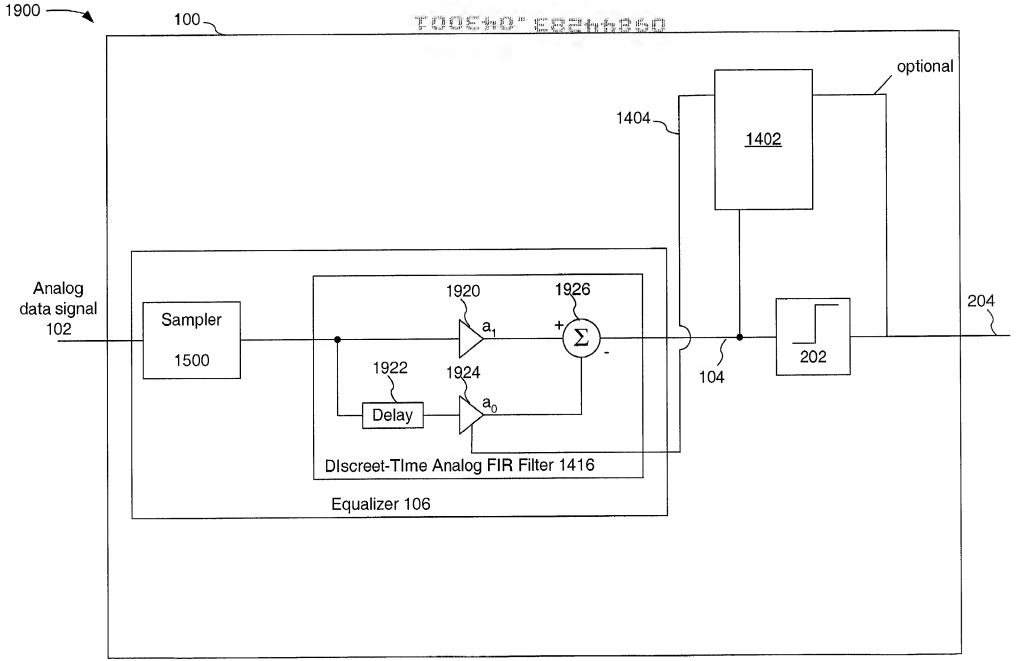


FIG. 19

0101-93.vsd/25

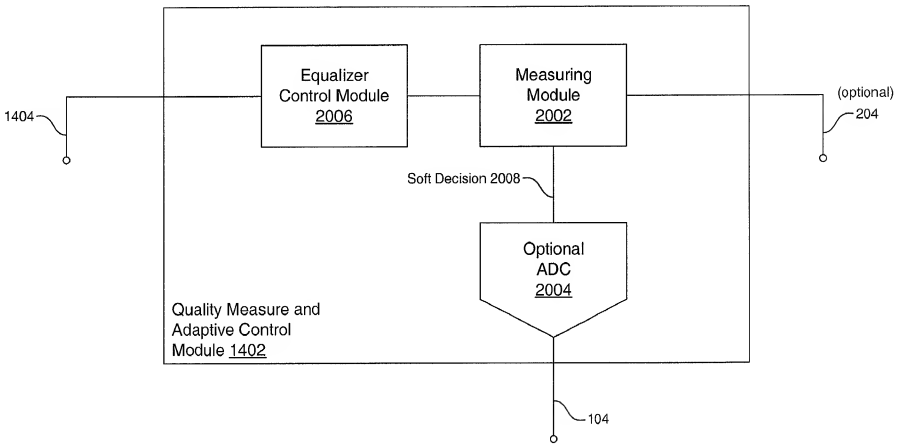


FIG. 20

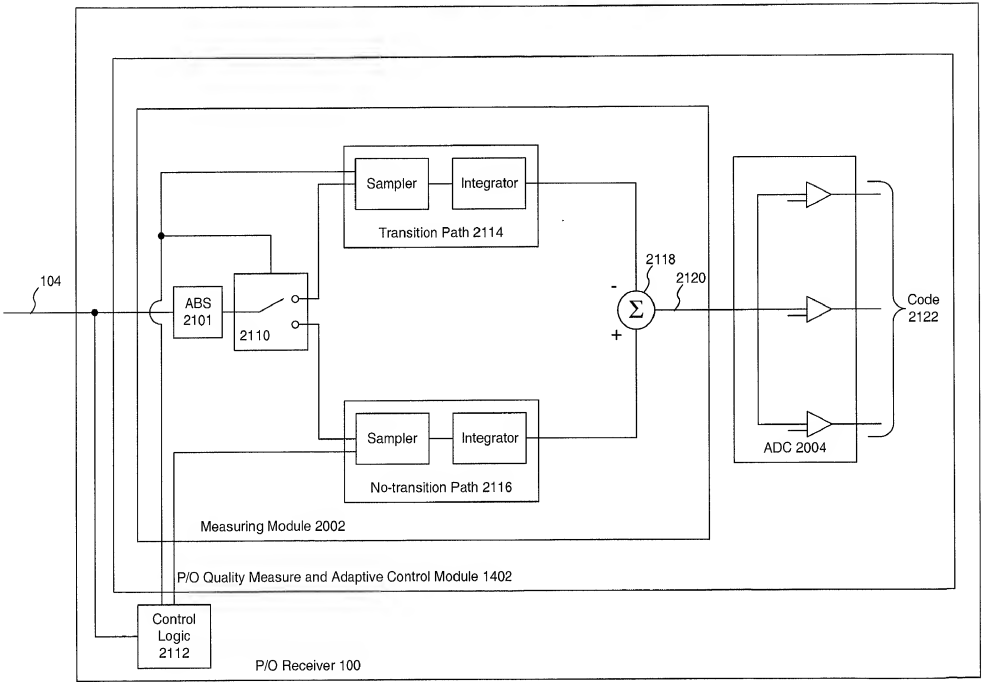


FIG. 21A

0101-93.vsd/27

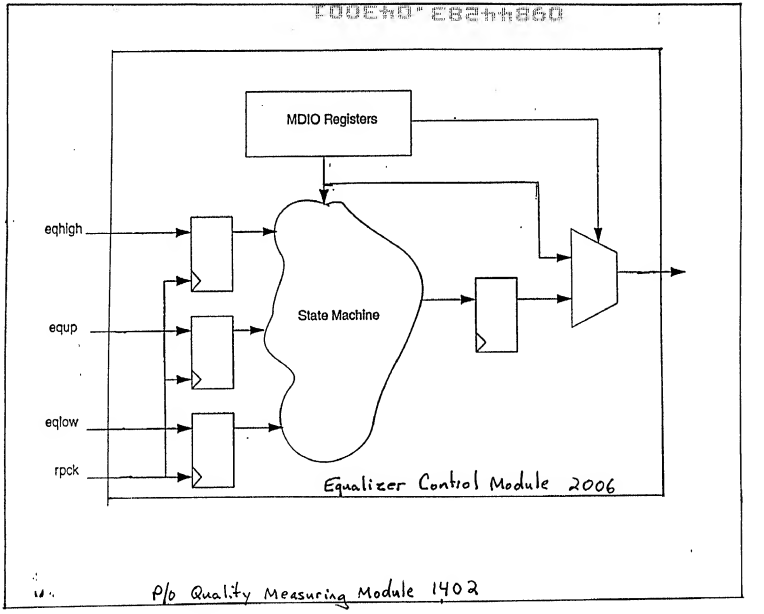

MDIO Registers
eqhigh
equp
eqlow
rpck
State Machine
Equalizer Control Module 2006
P/o Quality Measuring Module 1402

FIG. 21B

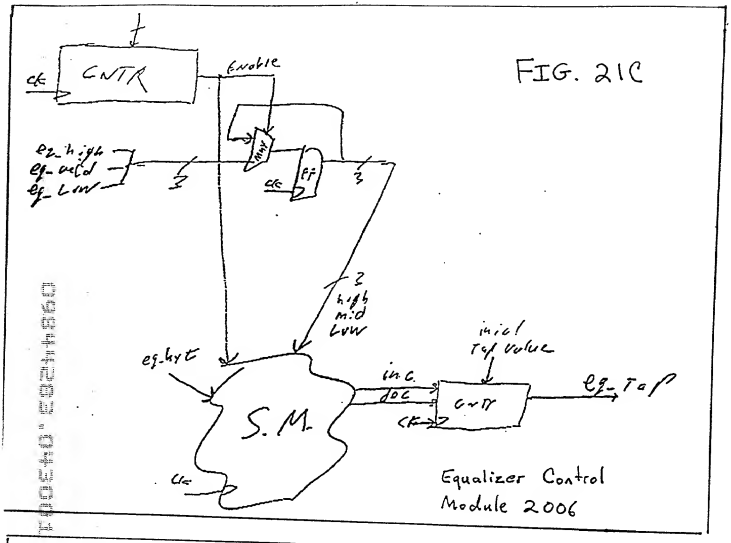


FIG. 21C

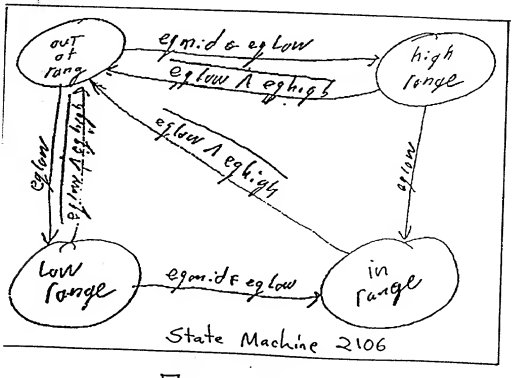


FIG. 21D

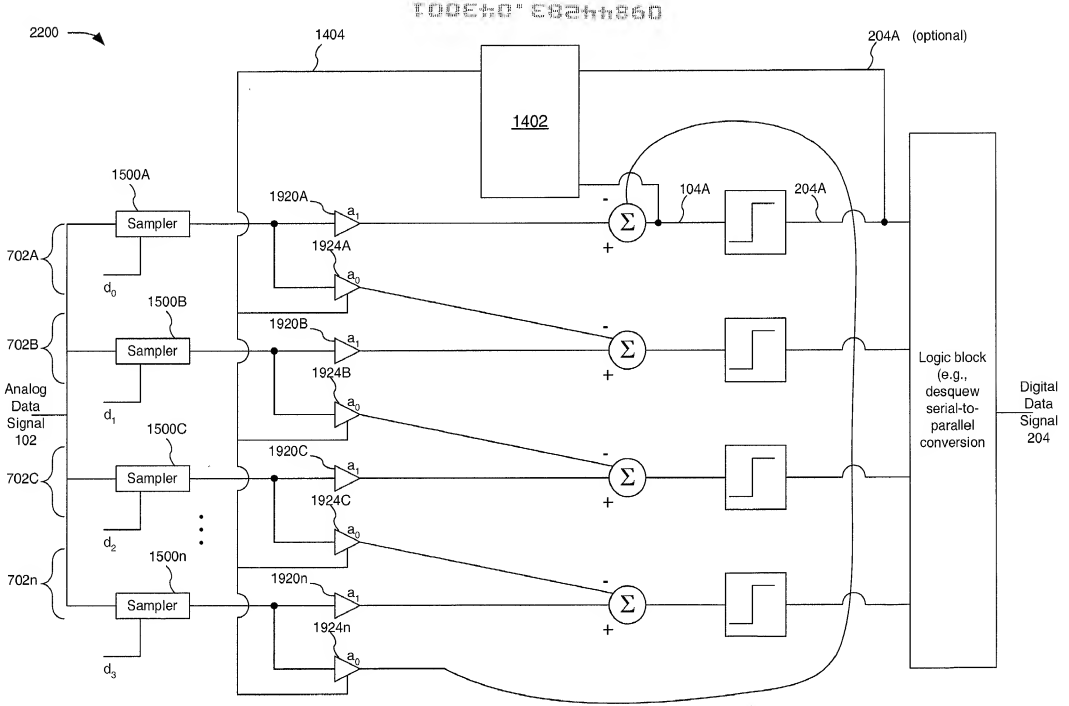


FIG. 22

0101-93.vsd/28

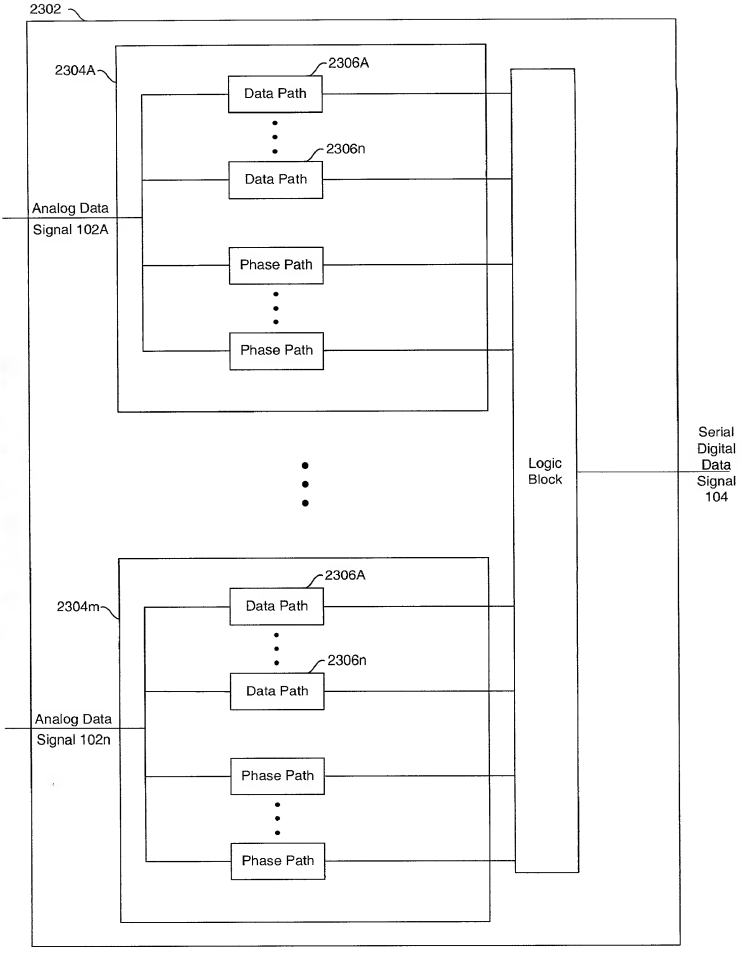


FIG. 23

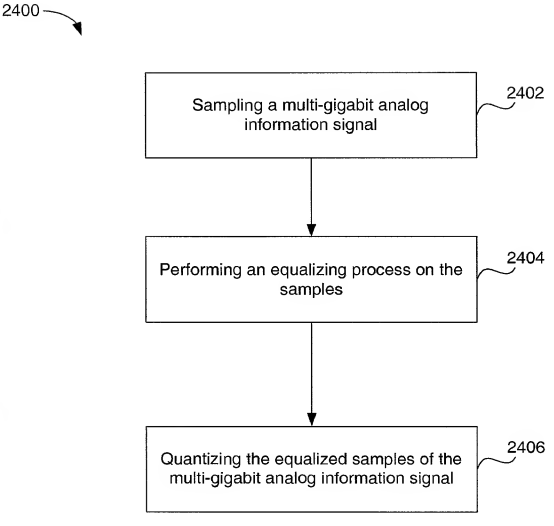


FIG. 24

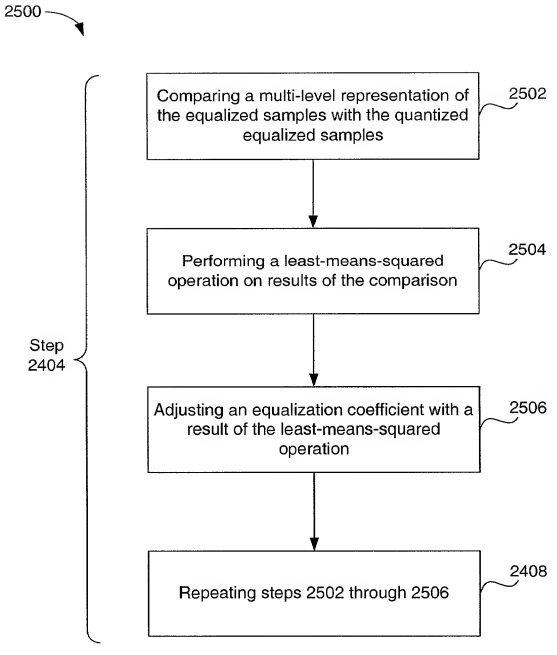

2500
Step 2404
Comparing a multi-level representation of the equalized samples with the quantized equalized samples
2502
Performing a least-means-squared operation on results of the comparison
2504
Adjusting an equalization coefficient with a result of the least-means-squared operation
2506
Repeating steps 2502 through 2506
2408

FIG. 25

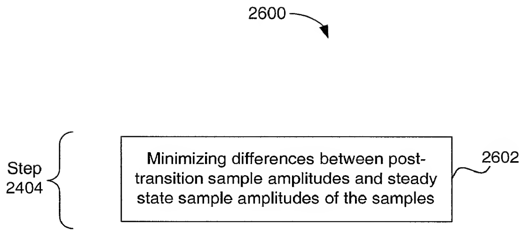

2600
Step 2404
Minimizing differences between post-transition sample amplitudes and steady state sample amplitudes of the samples
2602

FIG. 26

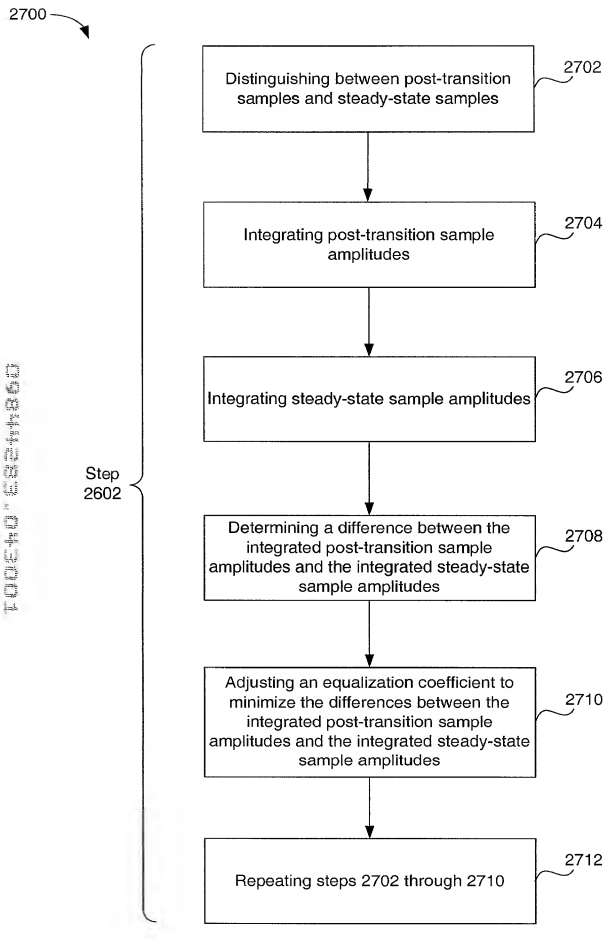

2700
Distinguishing between post-transition samples and steady-state samples
2702
Integrating post-transition sample amplitudes
2704
Integrating steady-state sample amplitudes
2706
Step 2602
Determining a difference between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2708
Adjusting an equalization coefficient to minimize the differences between the integrated post-transition sample amplitudes and the integrated steady-state sample amplitudes
2710
Repeating steps 2702 through 2710
2712

FIG. 27

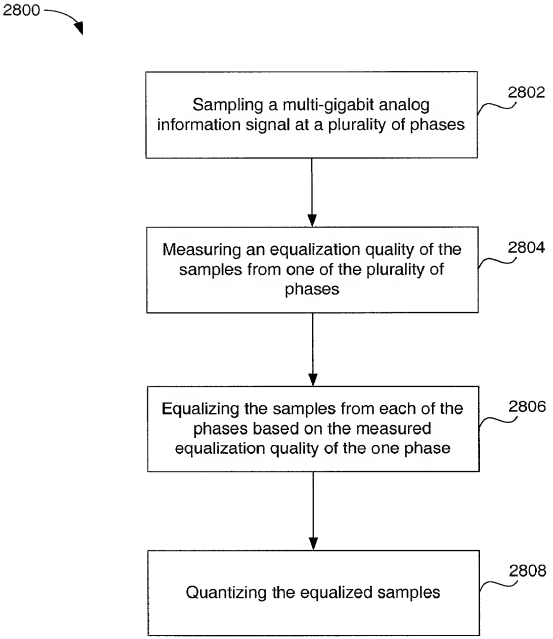

2800
Sampling a multi-gigabit analog information signal at a plurality of phases
2802
Measuring an equalization quality of the samples from one of the plurality of phases
2804
Equalizing the samples from each of the phases based on the measured equalization quality of the one phase
2806
Quantizing the equalized samples
2808

FIG. 28

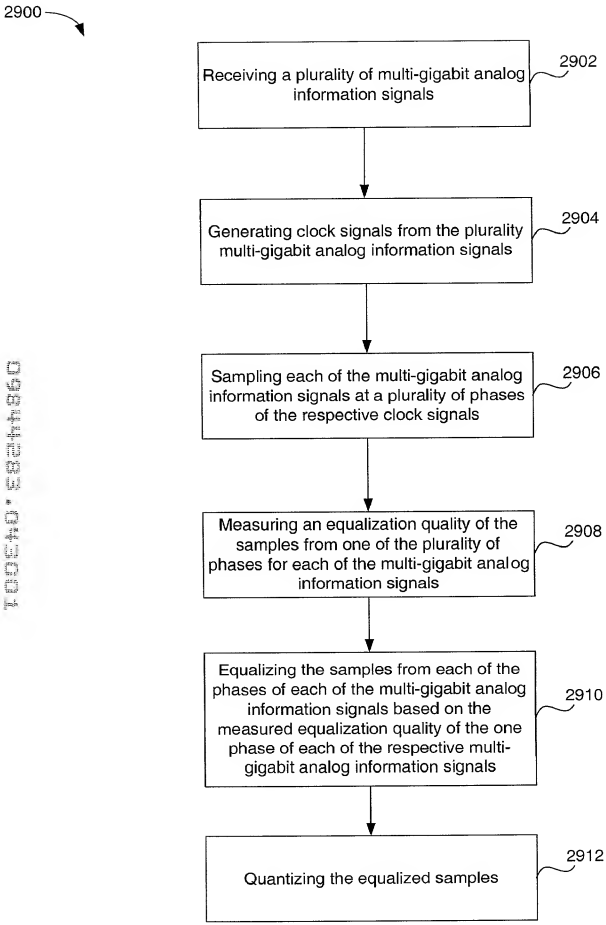


FIG. 29

0102-02.vsd/6

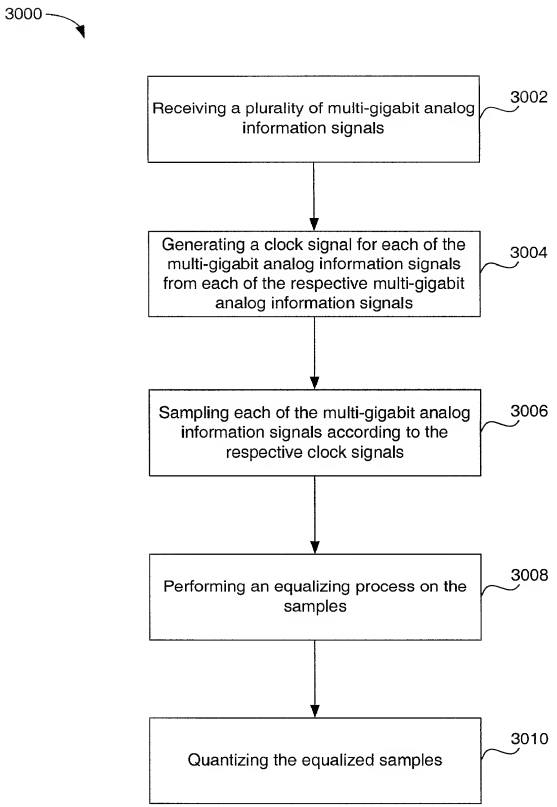

3000
Receiving a plurality of multi-gigabit analog information signals
3002
Generating a clock signal for each of the multi-gigabit analog information signals from each of the respective multi-gigabit analog information signals
3004
Sampling each of the multi-gigabit analog information signals according to the respective clock signals
3006
Performing an equalizing process on the samples
3008
Quantizing the equalized samples
3010

FIG. 30